REMARKS

At the time of the Final Office Action dated May 2, 2003, claims 4, 6, 9 and 12-19 were pending and rejected in this application. Claims 4, 6, 9 and 12-19 have been cancelled and new claims 20-26 have been added. Applicants submit that the present Amendment does not generate any new matter issue.

In the second enumerated paragraph of the Office Action, the Examiner objected to claims 6 and 17-18 for various informalities. As claims 6 and 17-18 have been cancelled, Applicants respectfully submit that the Examiner's rejection is moot.

CLAIM 12 IS REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY SEIDLER, U.S. PATENT NO. 4,780,098

Claim 12 has been cancelled, and thus the Examiner's rejection of claim 12 is moot. Applicants will therefore address the applied prior art of Seidler with regard to the newly presented claims.

Newly added independent claim 20 recites, in part, the following limitation: "at least one conductive member... covering a side surface of said semiconductor chip." This feature is shown, for example, in Fig. 4 of Applicants' disclosure. In the fourth enumerated paragraph on page three of the Office Action, the Examiner referred to Fig. 8 of Seidler and asserted that feature 260 corresponds to the claimed semiconductor chip and feature 210 corresponds to the claimed conductive member. As apparent from Fig. 8 of Seidler, the side surface (right side of

feature 260) of the substrate 260 is not covered by the lead 210. Instead, the lead 210 is positioned apart from the substrate 260. Thus, Seidler fails to identically disclose the claimed invention within the meaning of 35 U.S.C. § 102.

CLAIMS 4, 9 AND 13 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY TSUBOSAKI ET AL., U.S. PATENT NO. 5,714,405 (HEREINAFTER TSUBOSAKI)

Claims 4, 9 and 13 have been cancelled, and thus the Examiner's rejection of claims 4, 9 and 13 is moot. Applicants will therefore address the applied prior art of Tsubosaki with regard to the newly presented claims.

Independent claim 20 recites, in part, the following limitation: "a conductive member... covering a side surface of said semiconductor chip." In the fifth enumerated paragraph on page four of the Office Action, the Examiner referred to Fig. 9 of Tsubosaki and asserted that feature 1 corresponds to the claimed semiconductor chip and feature 3 corresponds to the claimed conductive member. As apparent from Fig. 9 of Tsubosaki, the side surface (right or left side of feature 1) of the semiconductor chip 1 is not covered by the lead 3. Instead, the lead 3 is positioned apart from the substrate 1 and separated from the substrate 1 by an insulating adhesive film 2. Thus, Tsubosaki fails to identically disclose the claimed invention within the meaning of 35 U.S.C. § 102.

CLAIM 6 IS REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY EIDE, U.S. PATENT NO. 6,014,316

Claim 6 has been cancelled, and thus the Examiner's rejection of claim 6 is moot. Applicants will therefore address the applied prior art of Eide with regard to the newly presented claims.

Independent claim 20 recites, in part, the following limitations: "at least a first electrode formed on a first major surface of said semiconductor chip; at least a second electrode formed on a second major surface of said semiconductor chip" and "said conductive member... covering a side surface of said semiconductor chip." In the sixth enumerated paragraph on page seven of the Office Action, the Examiner referred to Figs. 6a and 7 of Eide and asserted that feature 8 corresponds to the claimed semiconductor chip and feature 10 corresponds to the claimed conductive member. Although the Examiner did not identify with a corresponding reference numeral in Eide for the claimed first and second electrodes, the Examiner did assert that the first electrode is "under 10, the top" and the second electrode is "under 10, the bottom."

Unlike independent claim 20, which recites that the first and second electrodes are formed respectively on first and second major surfaces of the semiconductor chip, Eide fails to disclose this feature. The electrodes of Eide are shown, for example, in Figs. 1a, 1b and 2 as opposite extensions from the side surfaces of the IC/TSOP/TSOP package (1, 2, 3). Thus, the electrodes of Eide are not formed on the major surfaces. *Assuming arguendo* that one having ordinary skill in the art would consider the side surfaces of Eide as comparable to the claimed major surfaces, the top or bottom surface of Eide would not be considered comparable to claimed

side surface of Eide. Claim 20 recites that the side surface be covered by the conductive member, which the Examiner asserts is disclosed by feature 10 of Eide, but referring to Figs. 6a and 7 the top or bottom surface of the chip 8 is not covered by feature 10. Thus, Eide fails to identically disclose the claimed invention within the meaning of 35 U.S.C. § 102.

CLAIMS 14 AND 15 ARE REJECTED UNDER 35 U.S.C. § 102 AS BEING ANTICIPATED BY BERTIN ET AL., U.S. PATENT NO. 5,977,640 (HEREINAFTER BERTIN)

Claims 14 and 15 have been cancelled, and thus the Examiner's rejection of claims 14 and 15 is moot. Applicants will therefore address the applied prior art of Bertin with regard to the newly presented claims.

Independent claim 20 recites, in part, the following limitation: "said conductive member... covering a side surface of said semiconductor chip." In the seventh enumerated paragraph on page eight of the Office Action, the Examiner referred to Figs. 17 and 18 of Bertin and asserted that Bertin discloses a semiconductor chip 40A corresponding to that claimed. The Examiner, however, did not assert that Bertin discloses a conductive member, and from review of Figs. 17 and 18, Applicants submit that Bertin does not disclose a conductive member corresponding to that claimed. Thus, Bertin fails to identically disclose the claimed invention within the meaning of 35 U.S.C. § 102.

CLAIM 16 IS REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON BERTIN IN VIEW OF MIYOSHI, ET AL., U.S. PATENT NO. 5,895,970 (HEREINAFTER MIYOSHI)

Claim 16 has been cancelled, and thus the Examiner's rejection of claim 16 is moot. Applicants will therefore only address the applied secondary reference of Miyoshi with regard to the newly presented claims, as Applicants have already addressed the primary reference of Bertin.

Independent claim 20 recites, in part, the following limitation: "said conductive member... covering a side surface of said semiconductor chip." Referring to Fig. 4 of Miyoshi, the side surface (right or left side of feature 21) of the semiconductor element 21 is not covered by the lead 23a. Instead, the lead 23a is positioned apart from the semiconductor element 21. Thus, Miyoshi fails to disclose this limitation found in independent claim 20.

CLAIMS 17-19 ARE REJECTED UNDER 35 U.S.C. § 103 FOR OBVIOUSNESS BASED UPON SEIDLER IN VIEW OF KITAHARA, U.S. PATENT NO. 5,440,452

Claims 17-19 have been cancelled, and thus the Examiner's rejection of claims 17-19 is moot. Applicants will therefore address only the applied secondary reference of Kitahara with regard to the newly presented claims, as Applicants have already addressed the primary reference of Seidler.

Independent claim 20 recites, in part, the following limitation: "said conductive member... covering a side surface of said semiconductor chip." Referring to Figs. 9(a-d) and 10(a-e) of Kitahara, the side surface (right side of feature 1) of the chip 1 is not covered by the

lead 3. Instead, the lead 3 is positioned apart from the chip 1, and at times, separated from the chip 1 by an adhesive layer 52. Thus, Kitahara fails to disclose this limitation found in independent claim 20.

Applicants have made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicants invite the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicants hereby respectfully request reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Scott D. Paul
Registration No. 42,984

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SDP/SAB:kap
Date: August 4, 2003
Facsimile: (202) 756-8087